



# The ISS On-Axis Silicon Array

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On behalf of the ISS Collaboration

# “UK-ISOL SRS” STFC Funded Project

On-axis silicon array, one of two parts of the construction project originally conceived around the TSR Storage Ring at ISOLDE-CERN – now two separate entities.

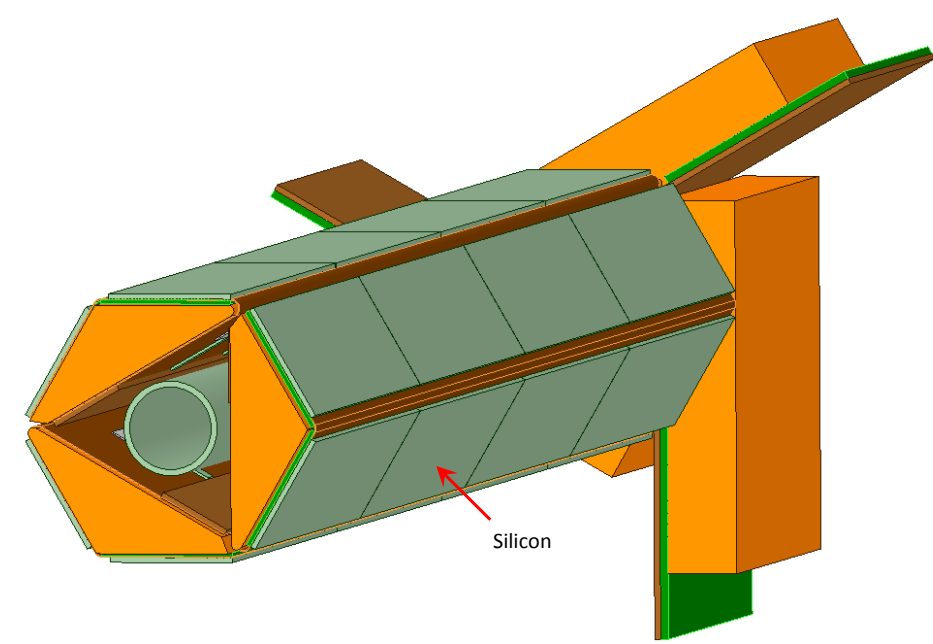
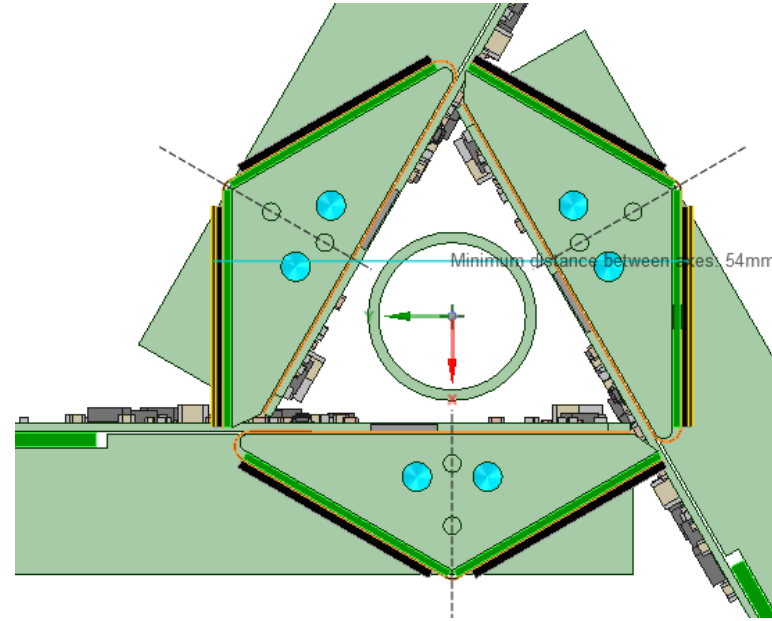
Work on the silicon array done by:

University of Liverpool, UK (Robert Page, Peter Butler, Jim Thornhill, David Wells and John Kenny)

STFC Daresbury, UK (Ian Lazarus, Alan Grant, Ian Burrows, Paul Morrall, Mike Cordwell, Marc Labiche)

# Overall design

Hexagonal geometry.  
Three modules make up array.  
Each has two rows of Si mounted on flex board. Wrapped around aluminum former. Three modules make up array.  
Si 25 mm from axis.  
0.5m long.



## *Double-sided silicon strip detectors:*

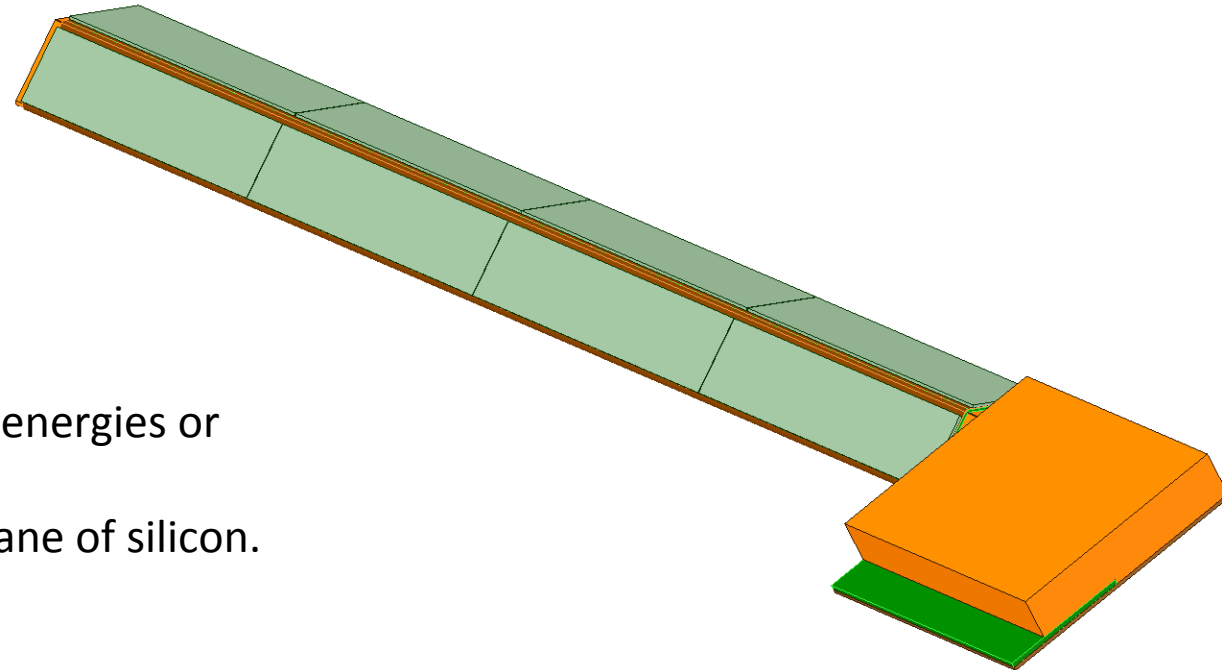
Strips parallel and perpendicular to beam axis.

Lower individual capacitance.

Simplified analysis – no need to correct for position-dependent energies or position non-linearity.

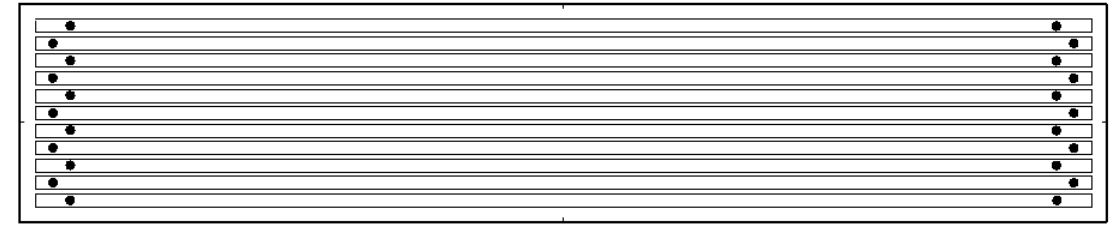
Reconstruct position on axis from interaction position on the plane of silicon.

Where charge sharing – perhaps get energies from other side?

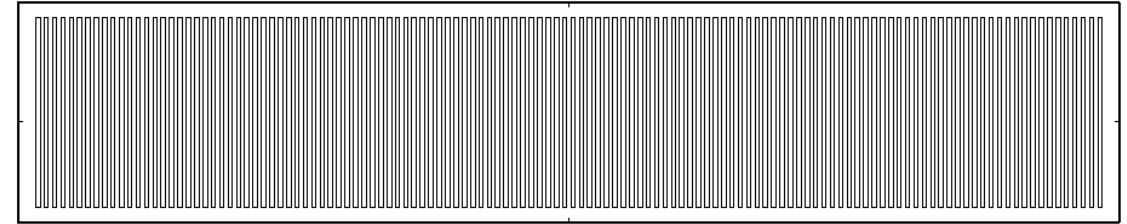


# Silicon wafers

DC-COUPLED DSSD	BB21(DS)-1000
Chip size	25mm x 125mm overall
Thickness	1000um
Full Depletion	150V typical, 250V max
Junction side	128 short strips, 0.953mm pitch, 100um gap
Ohmic side	11 long strips, 2.00mm pitch, 100um gap
Junction side Al	Bond pads 3000Å min, window 1000Å
Ohmic side Al	3000Å min
Junction contacts	Al bond pads both ends, side 100-200 um
Ohmic contacts	Gold finished, side 1800um
Total Leakage (20C)	3uA typical 5uA max
Total Capacitance	400pF typical



Ohmic (glue bonded)



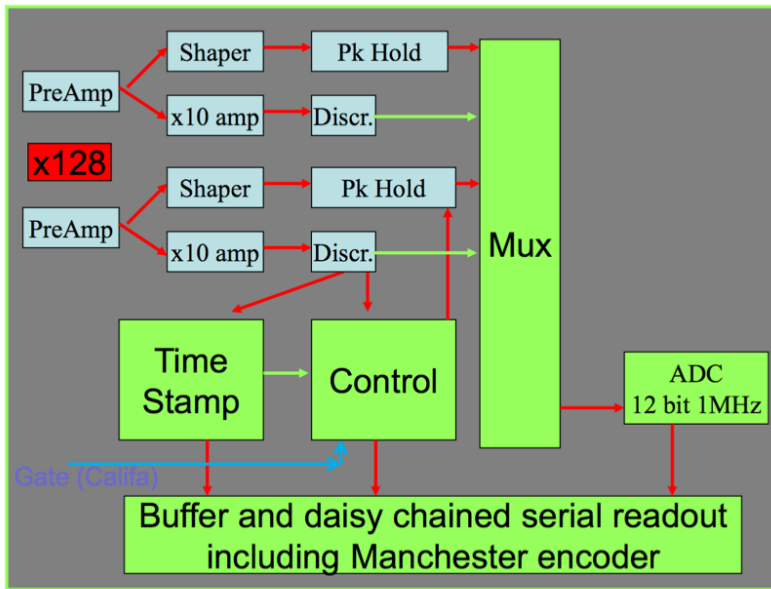
Junction (wire bonded)



**Figure 2** Photographs of double-sided silicon strip detectors. The top and bottom photographs show the full junction and ohmic sides, respectively.

# “R3B” ASIC

Time stamp  
Zero suppression  
On-chip ADC  
Serial readout



	<b>R3B ASIC</b>
<b>Energy Range (standard)</b>	0-50MeV
<b>Pitch of analogue inputs</b>	44um
<b>Size</b>	6.15 x 12.92mm
<b>Channels</b>	128
<b>Shaping amp</b>	CR-RC 0.5-8.5us. Reset with preamp after every hit.
<b>On chip ADC?</b>	Yes
<b>Output</b>	Serial data packets with daisy chain support.
<b>Threshold</b>	Adjust per chip. 1/10 range for both fast and slow thresholds (fine-tune per channel for matching)
<b>Input optimised for</b>	0-80pF
<b>Noise (specification)</b>	10keV rms, 40keV usable 50MeV range.
<b>Supports PSA?</b>	No
<b>Features</b>	On chip ADC/Mux reading only active channels. Time Stamp (5 or 10ns). Neighbour trigger logic (switchable). OR trigger out, Readout gate (optional) in.
<b>Pitch after modification</b>	100um
<b>Power dissipated</b>	1W per chip

# MODULES

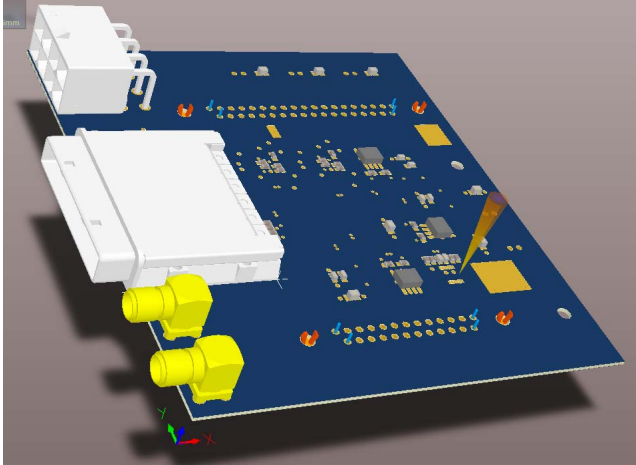


Figure 3 3D image of the external buffer PCB design.

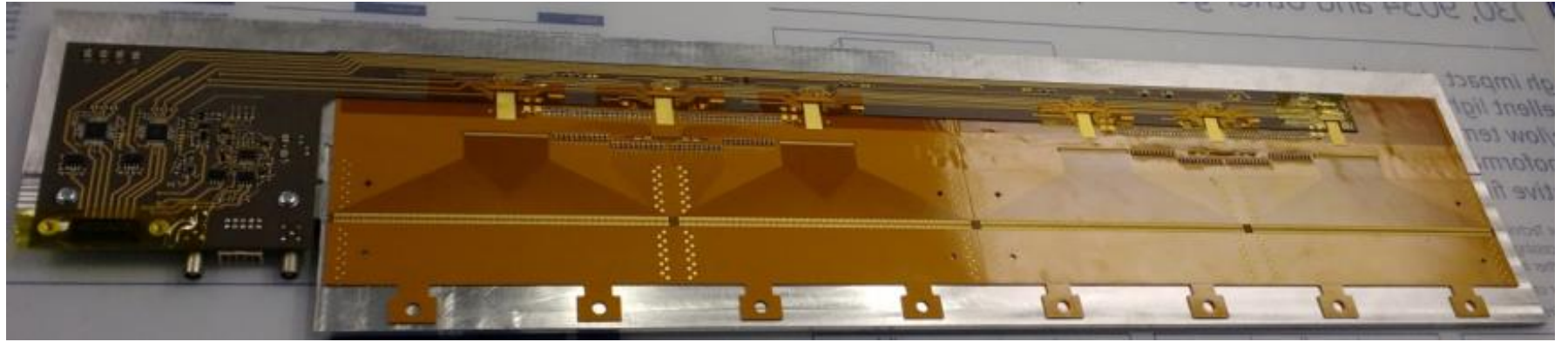


Figure 4 Two silicon flex PCBs fixed to an aluminium cooling plate and the L-shaped readout card attached over these to expose the pads for fixing the ASICs.

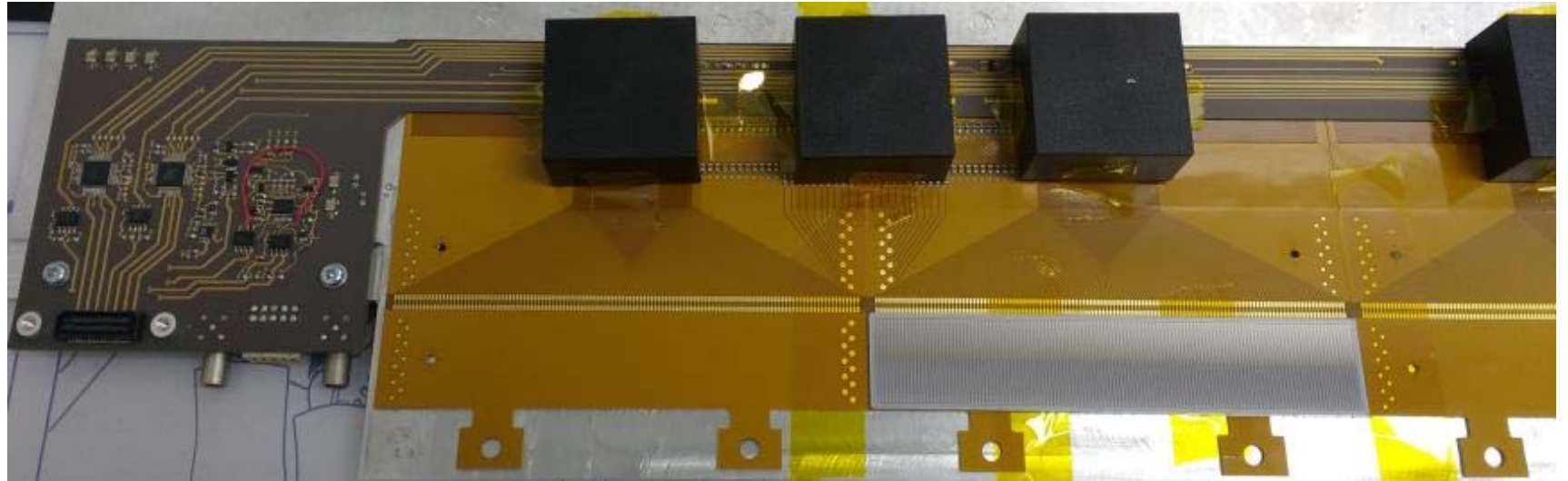


Figure 5 Test assembly with silicon attached with conductive glue to gold contact pads. The ASICs are under the protective black covers.

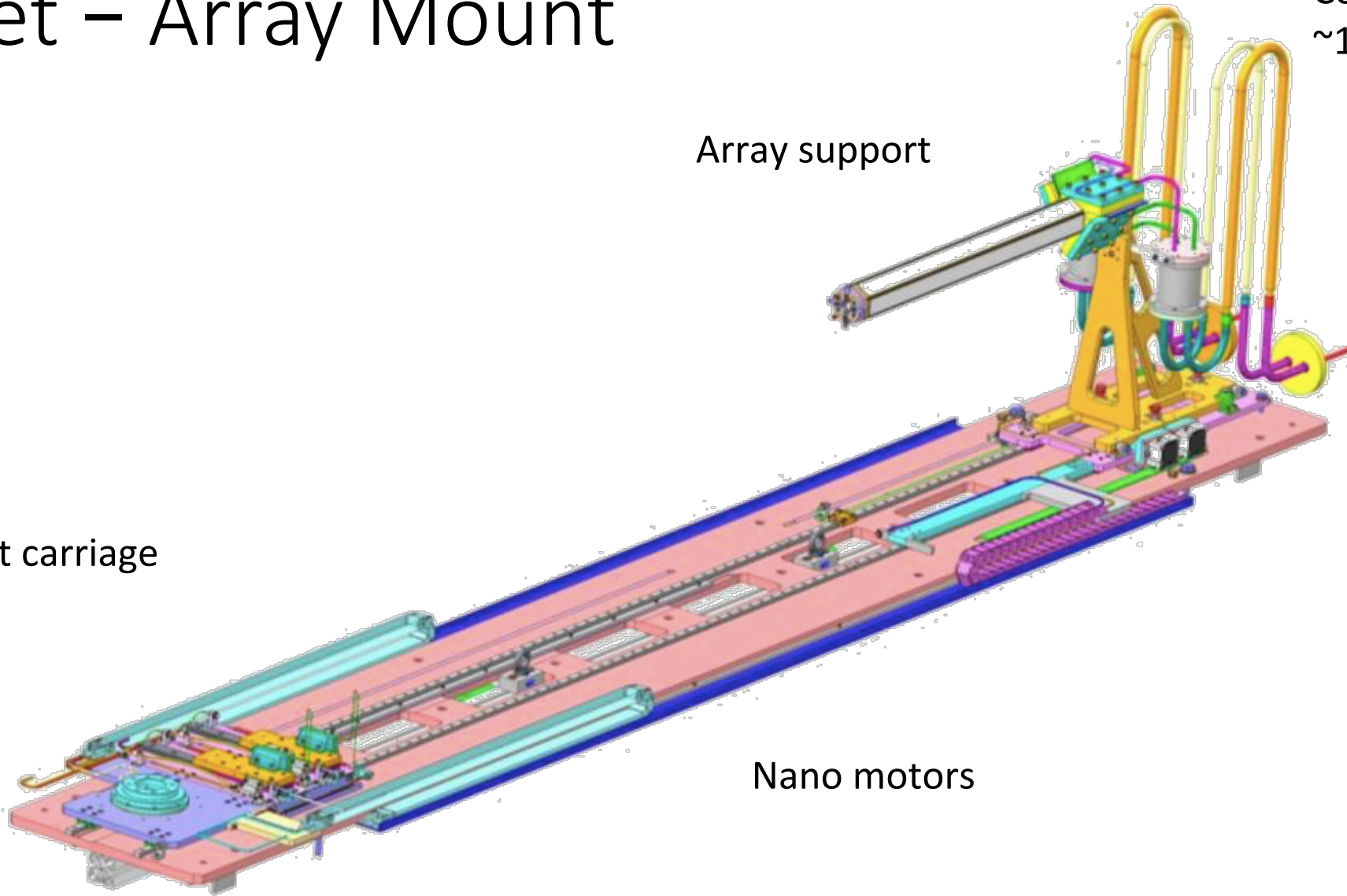
# Target – Array Mount

Cooling  
~13° rise along array.

Array support

Target carriage

Nano motors



# CURRENT STATUS

**SILICON:** first batch of 3 delivered in January after a manufacturing delay, acceptance tests in progress, a few teething troubles.

**SILICON MODULE, FLEX BOARDS, EXT/INT PCBS:** designs at final stages, prototypes available for vacuum testing, full manufacture soon. Bonding tests of ASIC successful

**TARGET-ARRAY MOUNT:** mechanical components of detector assembly, motor drive system and target delivered. Motion control specified. Design of target ladder, luminosity/monitors and silicon recoil mounts on going.

**EDAQ:** completed ready to use.

# FUTURE SCHEDULE

On track to be able to install completed array in 2019 at CERN during the Long Shutdown 2019 to early 2021. Testing with stable beams possible during this period.