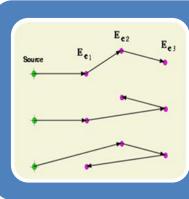
## Gretina DAQ

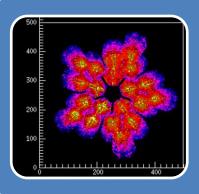
Chris Campbell LBL



#### Mode 1

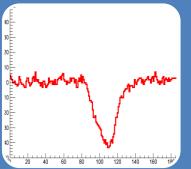
Tracked data

- Interactions grouped and ordered
- Includes Mode 2 data



#### Mode 2

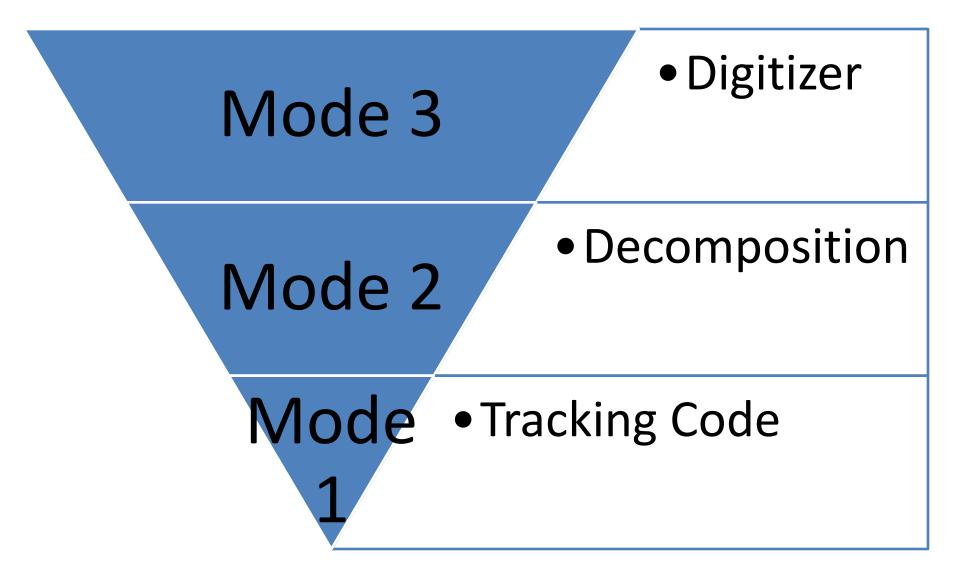
- Interaction points by crystal
- Crystal: Energy, position, time
- Interactions: Energy split and position in crystal



#### Mode 3

- Data organized by digitizer channels
- Header + waveform
- Header holds channel ID, filter data, time stamps

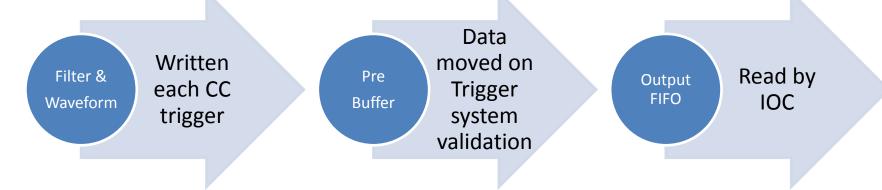
## Data Flow in Gretina





# Gretina Digitizer (LBL)

- Flash ADC
  - 100 MHz
  - 14 bit
  - 200 MB/sec of waveforms/channel
- Seven Gretina modules
  - 28 crystals
  - 40 channels/crystal
  - 1120 channels
- Full system waveform rate
  - 224 GB/sec
  - GRETA ~ 1 TB/sec
- So, we select the data!



## Gretina DAQ (I)

#### Each of the 28 crystals has:

- Separate VME backplane and IOC
  - Slow control in EPICS
  - Reads & timesorts digitizer data
  - Passes data to compute cluster
- 4 LBNL Digitizer Modules
  - 10 channels (9 segments + core)
  - 1 Flash ADC / ch, 14bit 100MHz
  - On-board FPGA filters
    - Energy (trapezoid)
    - Leading Edge (not CFD) (trigger primitive)
    - Pole-zero correction
    - Baseline Restoration
- Event data includes:
  - Timestamp
  - Filter data
  - Waveform subset



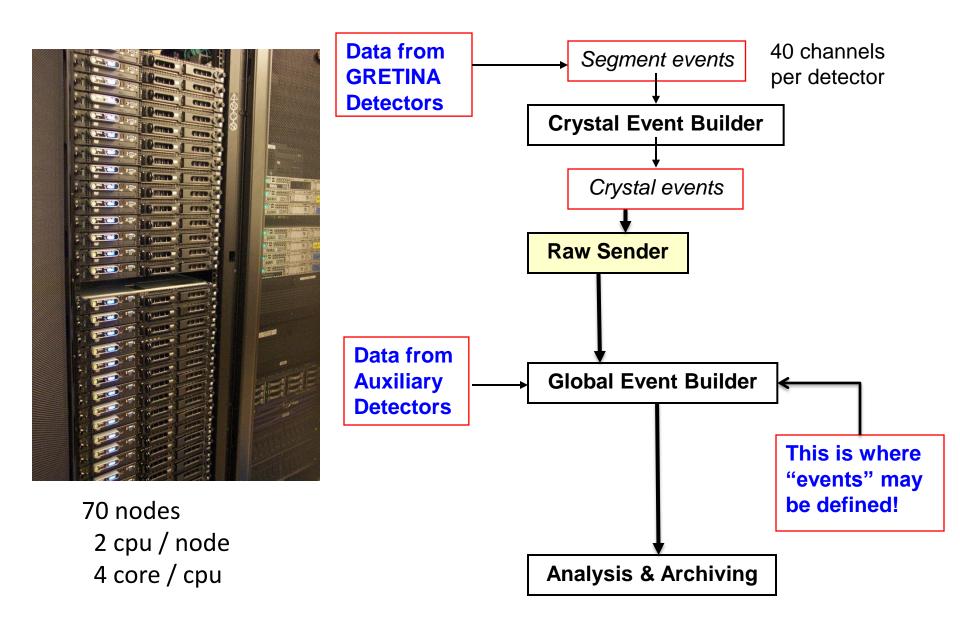
## Gretina DAQ (I)

#### Trigger system:

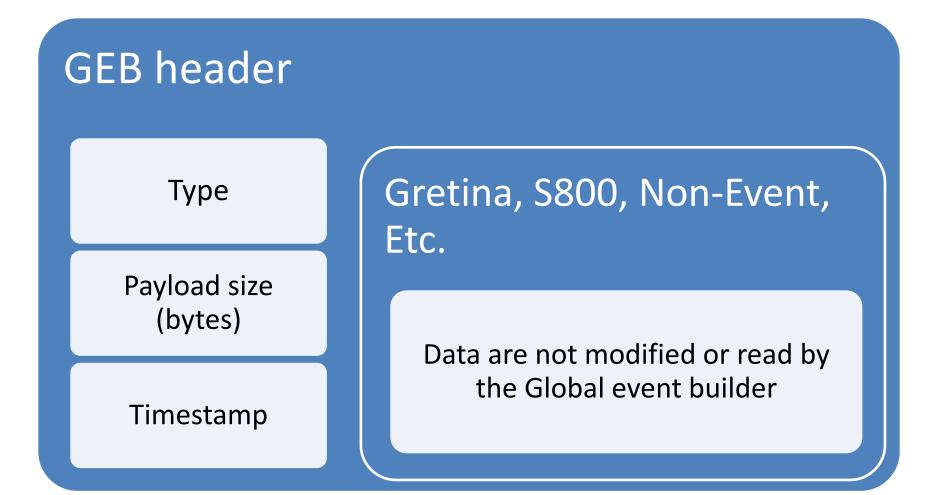
- 5 ANL Trigger modules
  - 1 Master + 4 Routers
- Master clock distribution
- Multiple trigger types
  - Multiplicity
  - External (coincidence)
  - Isomer
  - Sum Energy
- Event validation by timestamp broadcast
- NIM in/out interface with auxiliary DAQ available



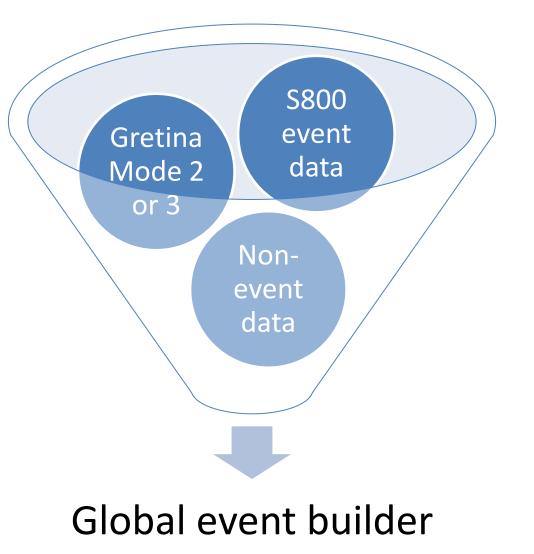
#### **Computing: Mode 3**



## GEB (Global Event Builder) packets



# Global event builder



- Data are sorted according to GEB header timestamp
- Sorted data is held until it is older than the newest data by a number of seconds.
- This correlation time is set by the user.
- GEB is a data bottleneck.

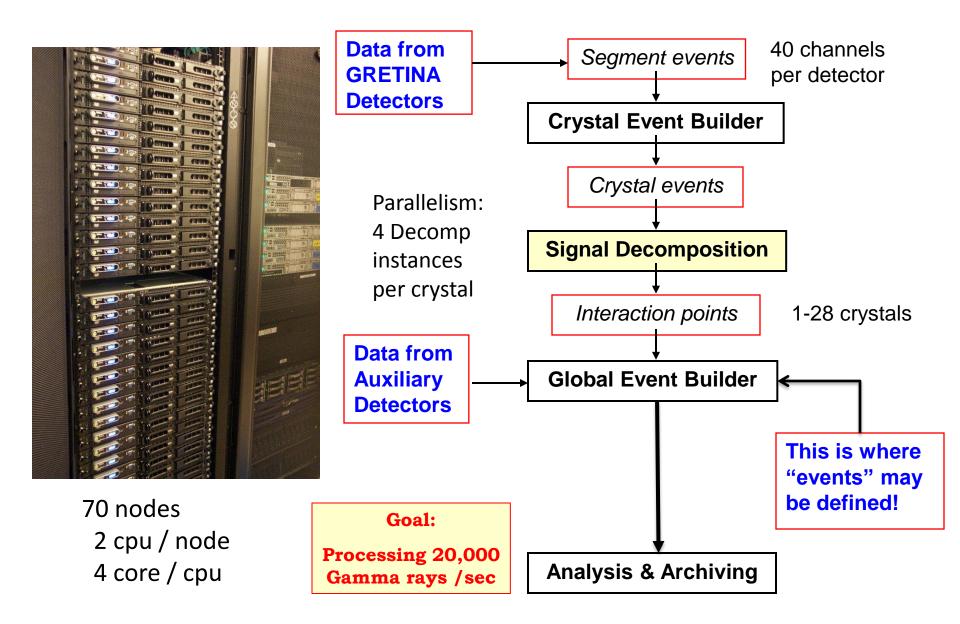
# Mode 3 data collection sub-types

- To eventually get Mode 2 (interaction positions)
  - Take data for all 40 channels for a triggered crystal
    - TTCS Mode
  - Collect ~ 2 $\mu$ s (200 samples) of waveform data centered on charge collection
  - Thus, 16kB/triggered crystal hit
- For energy calibration,
  - Read only hit (net charge) channels
    - Internal Mode
  - Collect minimal waveform, typically 6 samples for baseline
  - Typically, 200 300 B/triggered crystal hit

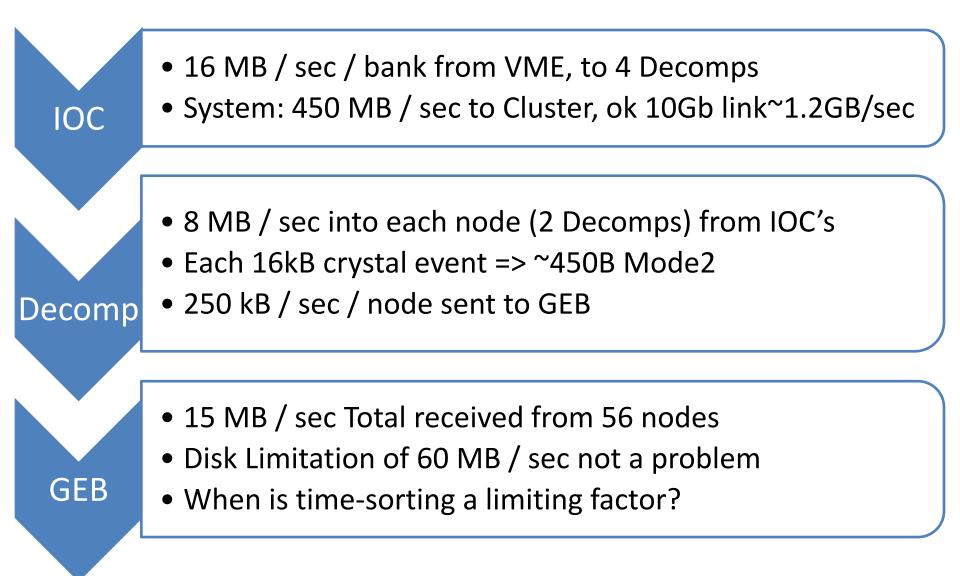
# Mode 3 to disk

- Limitations:
  - 1 MB output FIFO per Digitizer board
  - 20MB/sec total VME readout by IOC
  - 60MB/sec maximum sustained Gretina DAQ to disk
- Estimates:
  - Room Background
    - ~100Hz/crystal => 1.6MB/sec/crystal
    - 28 crystals => 45MB/sec
  - $-1\,\mu\text{Ci}$  source
    - ~600Hz/crystal => 10MB/sec/crystal
    - 28 crystals => 280MB/sec
- TTCS Mode 3 Calibrations are hard!
  - Imposed dead time system implemented by toggling trigger
  - OR, downscale the Gamma\_OR trigger

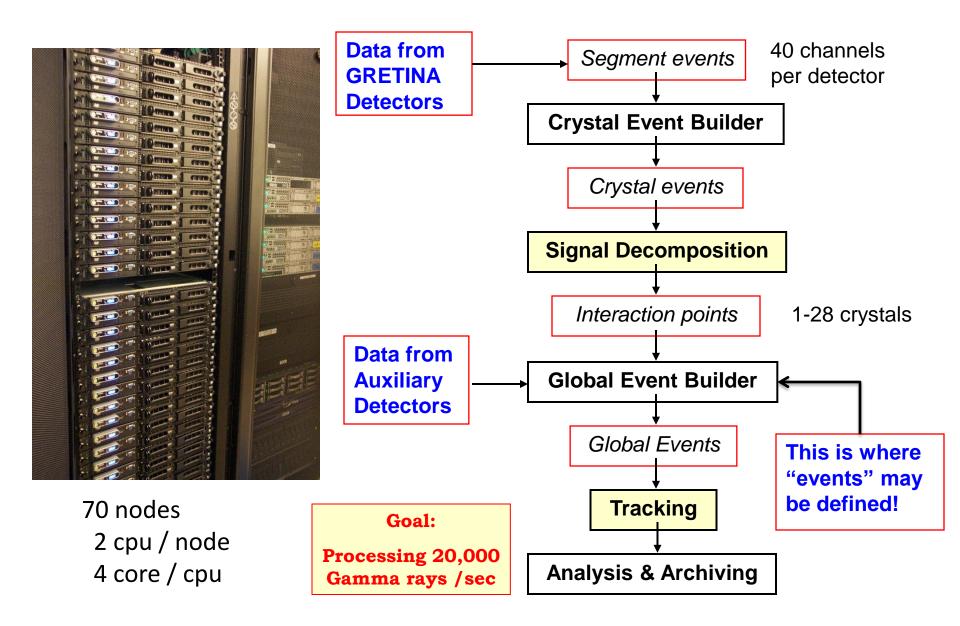
#### **Computing: Mode 2**



# Mode 2 Data Flow for 1kHz/crystal



#### **Computing: Mode 1**



# Auxiliary detectors

- Minimum requirement: synchronize + trigger
  - Timestamp
    - Added to Auxiliary DAQ, e.g. using a scaler
    - Gretina provides 50MHz clock and IMP SYNC (clock reset)
  - Trigger
    - Made in GRETINA trigger system and sent out
    - OR, Made externally and sent to GRETINA trigger system
- Merge data streams:
  - Auxiliary DAQ can output to the Global Event Builder directly
  - OR, File merge
    - DAQs write independent data files
    - Post-processing merges according to timestamps
- Can digitize Auxiliary detector triggers and timing signal(s) on Bank 29

#### Online DAQ Monitoring - GRETINA

X /global/devel/gretTop/11-1/tc	Dig/gretDigApp/Opi/U	serAlarms.edl			
GRETINA User Alarm Display			ImpSync received from Run Control?	Missing ImpSync	
			Gretina Timestamps internally synced?	Synced	
			Digitizer Board output FIFO status:	FIFO Overflows	
			Crystals Enabled:	28	
			[GEB] Cluster State		Setup
Crystal rates (in Hz)				Alarm Settings	
	Average	Min	Max	Min	Max
CC2 LED triggers	0	0	0	0	5000
CC2 Data Packets	0.0	0.0	0.0	0	5000
Decompositions	-1	0	0	0	1000
	Total		Time (sec)		
FIFO Overflows:	16101	Total Rur	Total Run: 285172.2		
Dead Time:	0 %	Inhibited	880.0		
Timestamps	Master Boards		May Di	fforonco	
	Min	Ma	x Difference	Max Difference Within a Bank	
Live (sec)	285318	28531	9 0.9		0.0
Latched 112229619938		11222961993	8 0		0

Key information has been distilled into one meaningful alarm page.

Digitizer timestamp synchronization tested every 10 seconds.

Scripts/Buttons allow users to recover from problems

# Problems:

- Digitizer stability
  - Firmware failures requiring FPGA reset
    - Run stop, Reset settings, Run start
  - Rate dependent failure above a few kHz per crystal with current firmware @NSCL
    - Higher rates ran stably under a previous version
    - Some compile dependence
  - Firmware is NOT software: clock jitter
    - Fixes will involve programming and hardware changes
  - Full DAQ (112 digitizer system) needed to test "system" failure rate
- IOC network failure
  - Failure one IOC (of 28 in system) per 1-2 days
    - Run stop, Reset settings, Run start
  - Under investigation
- High rates and segment summing
  - Both need digitizer firmware changes to run without losses

# Digitizer FPGA features implemented – to be tested

- Fixed-time energy pick-off
  - Instead of peak-find energy, might improve resolution
- Baseline restorer (BLR) changes
  - Vary time constant to minimize noise contribution
  - Inhibit window based on CC\_LED, not local LED, to lower the effective segment energy threshold
  - Inhibit window re-triggering (for high rates)
- Longer noise window
  - Inhibit spurious triggers

# **FPGA** improvements

- High rate dead time
  - Due to singular pre-buffer, only one event can be constructed and held for trigger validation at a time
  - Led to external trigger workaround at BGS
  - Better solution possible IF max trigger latency allows
- Serdes improvement
  - Digitizer to Trigger communication of "slow data"
  - Necessary for more advanced trigger conditions
    - Sum Energy Will this be used during ATLAS campaign?
- Shifted validate window to select trigger validations with a known time delay
- Digitizer timing MUX replacement to reduce clock jitter and improve code stability
- Add data to output format? (baseline, Trigger TS)

# Questions for users?

- What trigger conditions will you need?
  Is sum energy needed?
- What trigger rate and latency can we expect from your auxiliary detector?
- What auxiliary detector data size and rate will be sent to GEB? At what latency?
- What crystal rate and readout rate are expected?