



# E906 Trigger

R. Gilman, Rutgers University

Fermilab E906 Collaboration Meeting  
20 June 2008

# Apologies

- My apologies for not making the meeting, just out of organizing 4 days of meetings, and need the day to get ready for next week's trip

# Overview

- This talk is a small update on what was presented during E906 meeting in Dec 2006
  - Discussion largely unchanged, but solution is now cheaper...
- Based on discussions with
  - Reimer, Gagliardi et al NIM paper on E866 trigger, and with
  - Ed Bartz (Rutgers designer, worked on LHC FPGA projects for our high-energy group)

# Scintillator Tracks

- 8 hodoscope planes, each with 2 rows of 16 paddles, for a total of 256 signals
- Full specification requires detailed Monte Carlo (not done!), but scope of problem is about as follows:
  - Track in either X or Y would involve about  $32 \times 6 \times 6 \times 6 = 6912$  possibilities in each direction
  - Some of these do not point back to target
  - Similar number of possibilities for missing hit “efficiency tracks”

# Scintillator Triggers

- Triggers involve correlating x and y to form tracks
  - Primary trigger: two tracks,  $\mu^+$  and  $\mu^-$ , high  $p_T$
  - Various secondary triggers: two same sign  $\mu$ 's, one track, cosmic track, noise

# E866 Trigger

- Trigger logic largely implemented using numerous LeCroy programmable units based on Xilinx Field Programmable Gate Array (FPGA) chip
- Identify in each direction quadrant of track in 1<sup>st</sup> plane, side of spectrometer, position in 4<sup>th</sup> plane, sign (for bend direction)
- Technology modern as of ~15 years ago; now we can do better

# Modern FPGAs

- FPGA chip technology has improved - as of 12/2006, for example
  - Xilinx Virtex5 family has up to 500 Mhz speed, ~1000 input/outputs, few hundred thousand logic elements (6-input look-up tables)
- After a few hours of discussion with Ed Bartz, he expects we can do the entire trigger logic on a single chip

# Interface with CODA DAQ

- Plan: FPGA system would
  - have input from all 256 paddles
  - generate several trigger types
  - send the several trigger bits to CODA trigger supervisor for prescaling, etc, and to scaler for counting



# Cost and Schedule as of 12/2006


Design	\$50,000.00	Sep 2007	6 months
Prototype	\$26,000.00	Mar 2008	6 months
Test	\$13,000.00	Sep 2008	2 months
Fabricate	\$14,000.00	Feb 2009	1 month
Install	-	Apr 2009	1 month

- Estimate for custom system as of 12/2006
- But 1.5 years have passed, technology has advanced, prices have dropped
- Standard system now allows lower price and technological certainty

# CAEN V1495 FPGA

> CAEN > Nuclear Physics > Products > Front End > VME > I/O Registers > V1495

Login | Register



**CAEN**  
tools for discovery

**Nuclear Physics**  
Tools for discovery

Company Network

Sales Network

Contact us

Newsletter Area

**Nuclear Physics** | **Products** | Support | Custom Projects

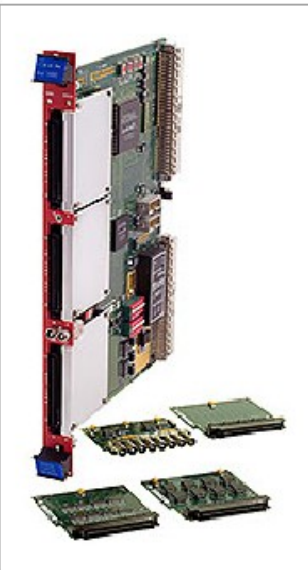
Search:  →

VME - V1495

General Purpose VME Board

**Products** ←

- Front End
  - VME
    - I/O Registers



**Highlights**

- User customisable FPGA Unit (with preloaded demo code)
- LVDS/ECL/PECL inputs (differential)
- 64 inputs, expandable to 162 (with 32 outputs)
- 32 outputs, expandable to 130 (with 64 inputs)
- 405 MHz maximum frequency supported by clock tree for registered logic
- I/O delay smaller than 15 ns (in Buffer Mode)
- Programmable 3-color LED

**V1495**

Technical Specifications Table

Manual

Software

Release Notes

Ordering Options

Printable Data-Sheet

2007 VME Catalog

**Compare with other products**

**Send this page** ←

# CAEN V1495 FPGA

- VME 6U board
- 64 - 162 inputs
- 32 outputs
- 405 Mhz max frequency
- I/O delay < 15 ns (in Buffer Mode)
- Cost ~\$3k for base unit

# Trigger Cost

- 3 CAEN V1495 FPGAs
  - Natural to have  $X$ ,  $Y$ , and  $X+Y$ , - but not necessary
- MiniVME crate
- Likely need to build conversion boards to convert format of scintillator discriminator / mean timer output to FPGA input
- About \$20 - 25k
- About 1 year of time for MC's and trigger programming development

# Where do we get the resources?

- About \$20 - 25k
  - Prof. TH Chang, Taiwan, will buy 1-2 FPGA boards as part of new grant
  - Rutgers can afford rest of system from ongoing NSF grant
- 1 FTE time
  - Student from Taiwan will come to Rutgers toward end of year to work on system
  - RU should have part time from Prof. Gilman and from one of postdocs + students

# Summary

- Project appears very achievable, on a time scale of ~1 year and cost (~25 k\$) mentioned
  - A fraction of the cost that we estimated 1.5 years ago