Master Trigger Module
May 16, 1995

1.0 OVERVIEW OF MASTER TRIGGER MODULE 3
1.1 Description of the Master Trigger Module 3
1.2 Block Diagram of the Master Trigger Module 4
1.3 Subsections of the Master Trigger Module 6
1.3.1 Front Panel Connectors 6
1.3.2 VXI Interface 7
1.3.3 Trigger Logic ECL PALs 7
1.3.4 Analog Adder and Comparator Circuits 10
1.3.5 ECL Digital Adder and Latches 11
1.3.6 ECL Lookup Table Interface 12
1.3.7 32 Bit Scaler FPGA 14
1.3.8 1 Usec Counter FPGA 14
1.3.9 External and Internal TDC 15
1.3.10 FASTOUT Data Controller FPGA 16
1.3.11 Dual Port RAM (DPR) 17
1.3.12 Pipeline Registers 18
1.3.13 VXI Local Bus Interface 18
1.3.14 Miscellaneous Circuitry 19
1.4 Memory Map for MTM 20

2.0 SCHEMATICS OF MASTER TRIGGER MODULE 27

3.O SCHEMATIC OF MTM's VXI INTERFACE FPGA 27

4.0 SCHEMATIC OF MTM'S FASTOUT FPGA 27

5.0 SCHEMATIC OF MTM's 32-BIT SCALER FPGA 27

6.0 SCHEMATIC OF MTM's ONE USEC COUNTER FPGA 27

APPENDIX A: ABEL PROGRAM FOR ECL PALs 27

APPENDIX B: TEST SOFTWARE 27

APPENDIX C: DATA SHEETS FOR PARTS USED IN MTM 27

HISTORY

Date	Who	What
5-3-95	John Weizeorick	Finalizing
1-3-95	John Weizeorick	Updated Memory Map and added more description
5-26-94	John Weizeorick	Original

1.0 OVERVIEW OF MASTER TRIGGER MODULE

This section gives a brief overview of the Master Trigger Module which was designed and developed by Argonne National Laboratory's Electronics Department, to meet LBL's specifications for the GammaSphere Project.

1.1 Description of the Master Trigger Module

The basic function of the Master Trigger Module is to determine when to generate a Master Trigger based on inputs form six Local Trigger Modules and/or a number of external inputs.

The trigger sequence is divided up into the Pre-Trigger, Main-Trigger, and the Late-Trigger phases. The Pre-Trigger phase must be entered before any Master-Triggers can be generated. A Master-Trigger is started, if the conditions are met, at the end of the Main-Trigger phase. The Late-Trigger phase can abort a Master-Trigger by sending an Inhibit signal to the Master Readout Module. When the Master Readout Module receives the Inhibit signal it generates an End of Event to all of the GeBGO Mother boards. A more detail description of these three phases are given below.

The **Pre-Trigger** phase is started when the programmable Pre-trigger condition is meet. This can be any boolean combination of the following three digital inputs.

Ge_Pre_Trg = True when the sum of the six analog Ge multiplicities from the six Local Trigger Modules are above the Programmable Ge Pre-Trigger Level.

Mod_Pre_Trg = True when the sum of the six analog Mod multiplicities from the six Local Trigger Modules are above the Programmable Mod Pre-Trigger Level.

Ext_Pre_Trg = An External input signal from a lemo on the front panel of the Master Trigger Module.

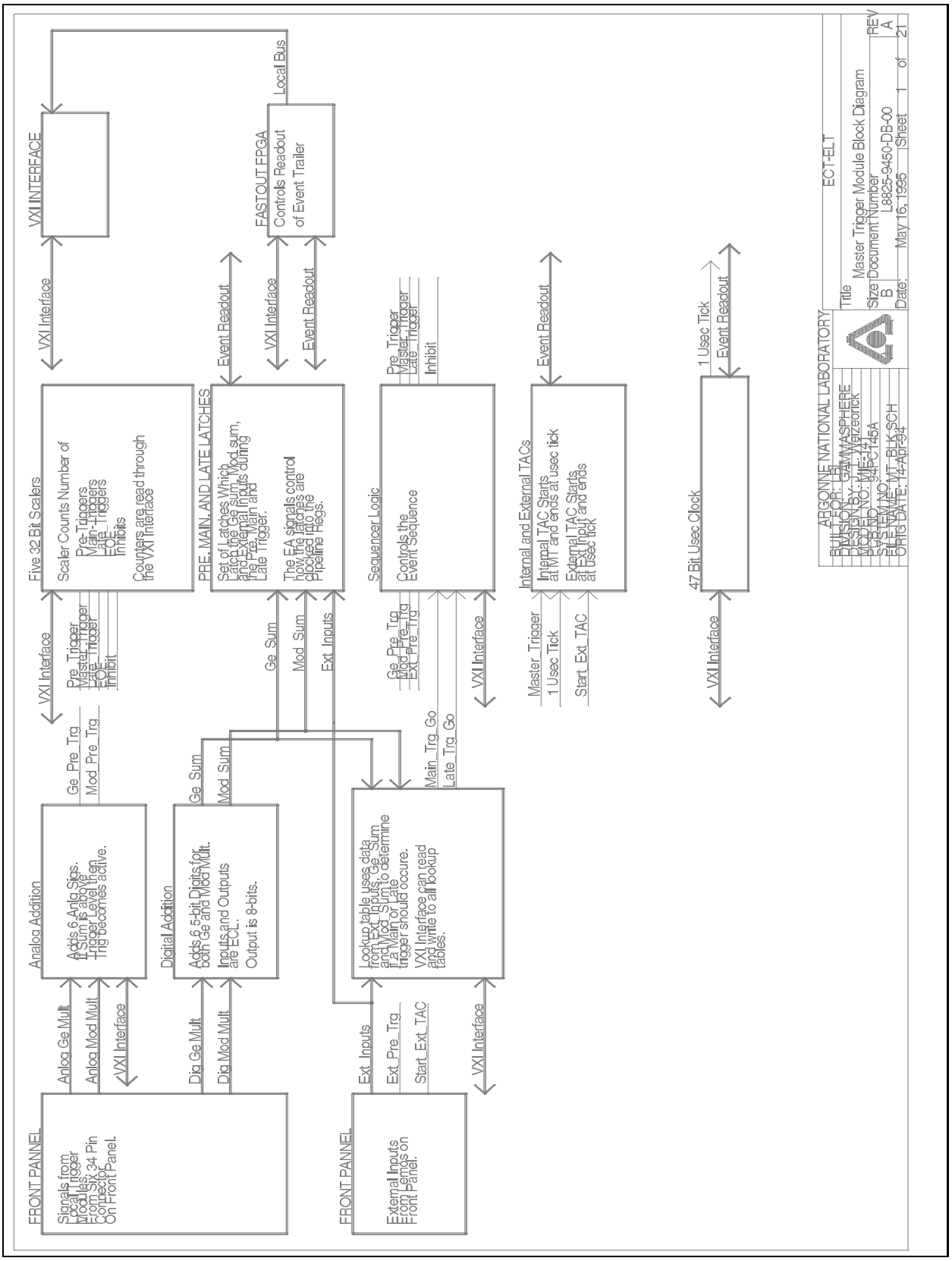
Once the Pre-trigger condition is met the Master Trigger Module generates a strobe pulse of programmable width, that goes to all of the Local Trigger Modules. The strobe pulse is used by each Local Trigger Module to trigger two ADCs which digitize the Ge and Mod and Multiplicities. On the falling edge of the strobe pulse the Master Trigger Module latches the digital sum of the Ge and Mod Multiplicities. This number can be read in the event trailer, which is put into the event data stream by the Master Trigger Module.

The **Main-Trigger** phase starts after a programmable delay from the Pre-trigger (300-400 nsec). Like the Pre-trigger, when the main-trigger is start, it sends a strobe pulse is sent back to the Local Trigger Modules which digitize the Ge and Mod multiplicities. On the falling edge the strobe pulse the Master Trigger Module latches the digital sums of the Ge and Mod multiplicities, which can be read in the event trailer. The Ge and Mod sums along with 8 external signals go into a Lookup table called the main Lookup table. This Lookup table is used to determine if a Master Trigger is to be generated. If the output of this Lookup table is high on the falling edge of the main strobe then a Master Trigger is generated.

The **Late-Trigger** phase only occur if a master trigger is generated. Like the Pre and main-trigger the late-trigger sends a strobe back to the Local Trigger Modules which digitize their Ge and Mod Multiplicities. On the falling edge of the strobe pulse the Master Trigger Module latches the digital sums, which is can be read in the event trailer. The Ge and Mod sums along with the 8 external signals go to the Late Lookup Table. This time the Lookup table is used to determine if the event sequence is to be inhibited or not. If the output is high on the falling edge of the late strobe then the event is successful and will be readout. If the output is low on the falling edge of the late strobe then the event has failed, and the event is inhibited. When an event is inhibited the Master Trigger Module sends out an inhibit signal to the Master Readout Module. When the Master Readout module receives the inhibit signal it generates an EOE (End of Event) which clears the data from the GeBGO Mother boards.

1.2 Block Diagram of the Master Trigger Module

On the following page is a block diagram of the Master Trigger Module. Section 1.3 describes the function of each section shown in the block diagram.


VXI INTERFACE
VXI Interface
Local Bus
FASTOUT FPGA
Controls Readout
of Event Trailer
Event Readout
VXI Interface
Event Readout
Five 32 Bit Scalers
Scaler Counts Number of
Pre-Triggers
Main-Triggers
Late Triggers
EOE
Inhibits
Counters are read through
the VXI Interface
PRE, MAIN, AND LATE LATCHES
Set of Latches Which
Latch the Ge Sum, Mod sum,
and External Inputs during
the Pre, Main and
Late Trigger.
The FA signals control
clocking of the
pipeline Regs.
Sequencer Logic
Controls the
Event Sequence
Pre_Trigger
Master_Trigger
Late_Trigger
Inhibit
Internal and External TACs
Internal TAC Starts
at MT and ends at usec tick
External TAC Starts
at Ext Input and ends
at usec tick
Event Readout
47 Bit Usec Clock
1 Usec Tick
Event Readout
VXI Interface
VXI Interface
Pre_Trigger
Master_Trigger
Late_Trigger
EOE
Inhibit
Ge_Pre_Trg
Mod_Pre_Trg
Ge_Sum
Mod_Sum
Ext_Inputs
Ge_Pre_Trg
Mod_Pre_Trg
Ext_Pre_Trg
VXI Interface
Master_Trigger
1 Usec Tick
Start_Ext_TAC
Analog Addition
Adds 6 Anlg Sigs.
If Sum is above
Trigger Level then
Trig becomes active.
Digital Addition
Adds 6 5-bit Digits for
both Ge and Mod Mult.
Inputs and Outputs
are ECL.
Output is 8-bits.
Ge_Sum
Mod_Sum
Lookup table uses data
from Ext Inputs, Ge Sum,
and Main or Late to determine
if trigger should occure.
VXI Interface can read
and write to all lookup
tables.
Main_Trig_Go
Late_Trig_Go
Anlog Ge Mult
Anlog Mod Mult
VXI Interface
Dig Ge Mult
Dig Mod Mult
Ext_Inputs
Ext_Pre_Trg
Start_Ext_TAC
VXI Interface
FRONT PANNEL
Signals from
Local Trigger
Modules
From Six 34 Pin
Connector
On Front Panel.
FRONT PANNEL
External Inputs
From Lemos on
Front Panel.
ARGONNE NATIONAL LABORATORY
ECT-ELT
Title
Master Trigger Module Block Diagram
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B
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1.3 Subsections of the Master Trigger Module

The Master Trigger Module (MTM) consist of the following subsections listed below.

- Front Panel Connectors
- VXI Interface FPGA
- Trigger Logic ECL PALs
- Analog Adder and Comparator Circuits
- ECL Digital Adder and Latches
- ECL Lookup Table Interface
- 32 Bit Scaler FPGA
- 1 Usec Counter FPGA
- External and Internal TDC
- FASTOUT Data Controller FPGA
- Dual Port RAM (DPR)
- Pipeline Registers
- VXI Local Bus Interface
- Miscellaneous Circuitry

Each subsection is decribed in detail in the following sections.

1.3.1 Front Panel Connectors

On the Front Panel there are six 34 pin ribbon cable connectors, and 11 lemo connectors. Each 34 pin ribbon cable connector goes to a separate Local Trigger Module. The following differential signals are transmitted between the MTM and the LTM over the 34 pin ribbon cable connectors.

DG0 to DG4	-	Digitized Ge Multiplicity.
DM0 to DM4	-	Digitized Mod Multiplicity.
Strobe	-	The rising edge of this signal from the MTM makes the LTM digitize their Ge and Mod Multiplicities. This signal is identical for all LTMs.
MT	-	This is the Master Trigger Signal which comes from the MTM and goes to LTM. This signal is identical for all LTMs.
AGE	-	Analog Ge Multiplicity from the LTM's Ge Sum Bus.
AM	-	Analog Mod Multiplicity from the LTM's Mod Sum Bus.

Unused ribbon cable connectors on the MTM should have the shorting plug inserted. This insures that the differential digital data from the unused connector will be zero.

All of the lemo connectors are NIM voltage levels. The function of the 11 lemo connectors are listed below.

Ext_Pre	-	This input can be used as external Pre_Trigger signal into the MTM. The Signal is active an active low NIM voltage level.
Ext_Start	-	This input is used to drive the external TAC. The signal is an active low NIM voltage level, and is used as the start signal into the external TAC. The Master Trigger Signal is used as the stop to the external TAC. The value of the external TAC can be read in from the trailer data of each event.
Ext_Trg0 -> Ext_Trg7	-	These inputs allow external data to be used in the Main and Late trigger test. Note that the logic level is inverted before it goes into the Main and Late Lookup Tables.
Pre_Trigger	-	This output provides a way for external devices to receive the MTM's pre_trigger signal.

1.3.2 VXI Interface

The VXI Interface FPGA allows a VXI Resource Manager to setup, monitor and control everything on the MTM. The VXI Interface FPGA is a VXI Register Based Interface with Dynamic Configuration. For more details on the VXI Interface FPGA see the schematic specific to the Master Trigger Modules VXI Interface and the memory map for the MTM.

1.3.3 Trigger Logic ECL PALs

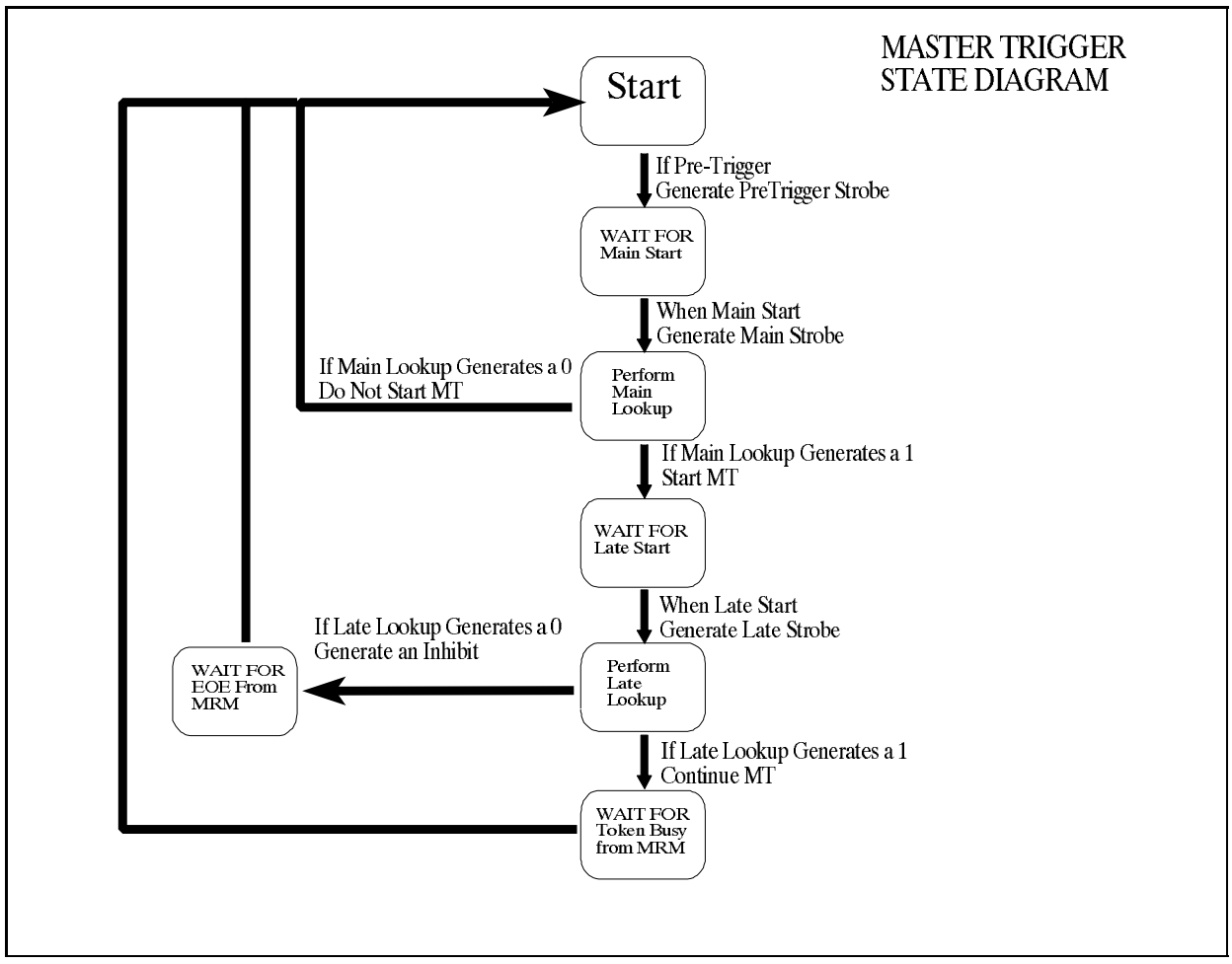
The trigger logic for the MTM is located in three decribed below ECL PALs.

PreTrigger PAL	-	The main function of this pal is to generate the Pre-Trigger signal. It uses the output from the Ge Multiplicity Comparitor, the Mod Multiplicity Comparitor, and the External PreTrigger Signal, along with six programmable mask bits to determine when the Pre-Trigger should be generated. The six programmable mask bits allow the user to pick any boolean combination of the Ge, Mod, and/or Ext-PreTrigger to generate a Pre-Trigger.
Sequential Logic 1 & 2	-	These two pals are used together to determine when to generate a Master-Trigger and when to inhibit the Master-Trigger.

The flow of a triggered event is decribed in detail in the State Diagram Shown Below. In addition to the State Diagram there are 6 timing diagrams showing the timing of the following events.

- Wave Form of a Signal Trigger
- Wave Form of a Signal Trigger with Inhibit
- Wave Form of a Double Trigger
- Wave Form of a Double Trigger with Inhibit
- Wave Form of Signals specific to the SEQ_LG1 PAL
- Wave Form of Signals specific to the SEQ_LG1 PAL

For the most complete understanding of the triggering logic the user must look at the ABEL programs used to program the three ECL PALs. These are given in Appendix A. The different versions of these programs are stored at LBL in the directory weizeor/man/mt_brd/pal.



Put timing diagrams here!

1.3.4 Analog Adder and Comparator Circuits

The two analog adder and comparator Circuits are used to generate two digital output. One output indicate when the Ge Multiplicity goes above a programmable multiplicity, and the other output indicates when the Mod Multiplicity goes above a programmable multiplicity. These outputs go to the Pre-Trigger PAL, where under program control, they can be used to generate the Pre-Trigger pulse.

The first analog adder takes the six Ge multiplicities form six Local Trigger Modules and adds them together. The second analog adder takes six Mod multiplicities form the six Local Trigger Modules and adds them together. The output of each analog adder goes into a separate comparator. The reference voltages can be varied from 0 to 2.56 volts by writing to two 8 bit DACs. Note that 0x00 = 0 volts and 0xff = 2.56 volts. To determine how to set the reference voltage for a specific multiplicity, lets follow the voltage levels through the system.

Each GeBGO Mother Board Applies 5 mA into 25 ohms for a Ge or Mod event. This means that we get 125 mV per event on the Sum Bus of each VXI Mainframe. The LTM buffers the sum bus and transmits it to the MTM. While the signal is sent to the MTM it is divided by 2. The MTM takes the signal, inverts it and multiplies it by 2. This means that into the adder we have -125mV per event. The adders take the voltage form all of the LTMs, sum them together and multiply the results by 2. This makes the output of the adder going into the comparator generate 250 mvolts per event. When the reference voltage going into the comparator is programmed for n multiplicity it must be a voltage lower then then the desired multiplicity but higher then n-1 multiplicity. The table below gives the middle voltage for a PreTrigger to occur at a desired multiplicity.

Multiplicity	Decimal Number	Hex Number	Reference Voltage	Voltage from Adder
0	0	0x00	0	0 mV
1	13	0x0d	130 mV	250 mV
2	38	0x26	380 mV	500 mV
3	63	0x3f	630 mV	750 mV
4	88	0x58	880 mV	1000 mV
5	113	0x71	1130 mV	1250 mV
6	138	0x8a	1380 mV	1500 mV
7	163	0xa3	1630 mV	1750 mV
8	188	0xbc	1880 mV	2000 mV
9	213	0xd5	2130 mV	2250 mV
10	255	0xff	2560 mV	2500 mV

1.3.5 ECL Digital Adder and Latches

There are two ECL wallace tree digital adders. The first adder takes six 5 bit digital Ge Multiplicities form the six Local Trigger Modules, adds them together, and generates an eight bit result (The most significant bit of the eight bit result is inverted, so 0x80 equals zero). The second adder performs the same function for the Module Multiplicities. The adders are continuously adding any number that comes in, including any transitions. The numbers form the LTMs come from a flash ADC. The rising edge of the Strobe pulse, which goes to all of the LTMs, is used to start the ADC conversion. By the falling edge of the Strobe pulse the conversion, and addition and the ECL Memory Lookup has been completed.

During a typical event there are three Strobes sent to the LTMs from the MTM. First when the Pre-Trigger starts the Pre-Strobe is generated, then the Main-Strobe, and if a Master-Trigger is generated, then the Late-Strobe. The results from each addition, as well as the state of the eight external inputs, are latched on the falling edge of each Strobe. This data is then available in the Trailer of the event data. For information about the data format of the Event Trailer see section 1.3.11 through 1.3.13.

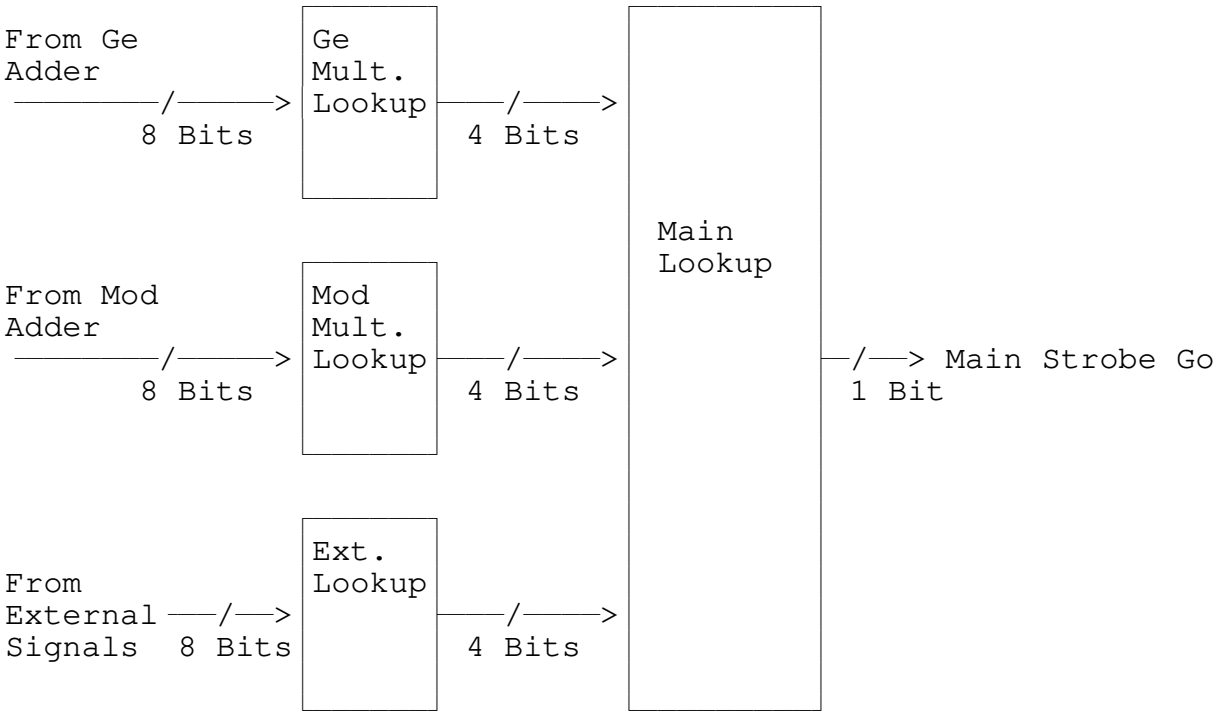
The results of the main and late Lookup provide an input into the ECL PALs, which control the event flow. The Adders, along with 8 external signals, provide the address lines into the Lookup tables. During the main strobe the main Lookup table is used, and during the late strobe the late Lookup table is used. For more details on the Lookup Tables see the next section.

1.3.6 ECL Lookup Table Interface

There are two sets of ECL Lookup tables. The first Lookup table is used during the Main-Strobe test, and the second Lookup is used during the Late-Strobe test. The ECL Lookup tables are ECL rams, which are mapped into the Master Trigger's VXI address space. They must be initialized for the desired trigger response. When the output of the Main Lookup Table is high, at the end of the Main-Strobe, it causes the Master Trigger to be generated. When the output of the Late Lookup Table is high, at the end of the Late-Strobe, it prevents an inhibit. This causes the token to be passed around and the event data to be collected.

The block diagram of the Main Lookup Table shows that the Lookup tables actually consist of 4 ECL Rams. After the block diagram there is a procedure that the VXI programmer can follow to initialize the ECL lookup Rams.

Main Lookup Table



1. Initialize the Main Ge, Mod and External Lookup tables. These are all programmed together by following the steps below.
   a. Write 0x11 into the **Lookup Table Control** Register. This selects the Main A0-7 D0-11 lookup table and directs the VXI to address the lookup tables. The same address will be given to all 3 lookup tables. The data written is split up so that the 4 ls bits go to the Ge Multiplicity Lookup Table, the middle 4 bits go to the Module Multiplicity Lookup Table, and the 4 ms bits of data will go to the External Lookup Table.
   b. Write zero into the **Lookup Table Address Pointer** Register. This will set the 8 bit address going to the Main A0-7 D0-11 lookup table to zero.
   c. Start writing 12 bit data into the **Lookup Table** Register. The address will be incremented each time a read or a write takes place. To initialize the entire table 256 writes will need to be done.

2. Initialize the Main Lookup Table
   a. Write 0x12 into the **Lookup Table Control** Register. This selects the Main A0-11 D0 lookup table and directs the VXI to address the lookup tables. Note that the data written into this ram is only one bit wide.
   b. Write zero into the **Lookup Table Address Pointer** Register. This will set the 12 bit address going to the Main A0-7 D0-11 lookup table to zero.
   c. Start writing 1 bit data into the **Lookup Table** Register. The address will be incremented each time a read or a write takes place. To initialize the entire table 4096 writes will need to be done.

3. Repeat the procedure above for the Late Lookup Tables

4. Write zero into the **Lookup Table Control** Register when finished initalizling the tables. This will allow the addresses into the Lookup tables to come form the adders and external signals.

1.3.7 32 Bit Scaler FPGA

The 32 Bit Scaler FPGA contains 5 32 bit scalers, with each scaler having a separate clock and gate. The contents of the scalers are mapped into the VXI memory and can be readout through the VXI bus. In the MTM the 5 scalers share a common reset and gate, which are controlled by setting and clearing two bits in the Miscellaneous Control Register. The counters are held in reset when the Reset bit is low, and the counters are gated off when the Gate bit is low.

Because the VXI interface for the MTM only allows 16 bit reads and writes, it takes two reads to get the contents of an individual scaler. In order to prevent ripple errors while reading the two words one may follow the steps below.

1. Read the most significant word.
2. Read the least significant word.
3. Reread the most significant word and verify that it has not changed.

If the most significant word has changed then a carry from the ls to ms word has occurred between reads and the 32 bit scaler number is not valid. The program must repeat the procedure to get a valid 32 bit number.

If a scaler is in the process of being incremented during a read, then the scaler will activate its SCALER_BSY signal. This will cause the read to be delayed, until the scaler has finished being incremented. This is done to insures that a word read over the VXI bus is not be in a transitional state.

The five signals going into the scalers:

1. Pre-Trigger - Generated every time there is a Pre-Trigger
2. Master-Trigger - Generated every time there is a Master-Trigger
3. Late-Strobe - Generated every time there is a Master-Trigger
4. End of Event - Generated by the MRM when an event is aborted. This can be due to an Inhibit from the MTM and when an event is not readout due to a WAIT signal from the VME.
5. Inhibits - Generated by the MTM when an event fails the Late-Strobe test.

See the section describing the Memory Map for the MTM to get the relative addresses of the five scaler listed above.

1.3.8 1 Usec Counter FPGA

The 1 usec counter FPGA consist of a 48 bit counter, that is incremented every 1 usec, and five 16 bit programmable registers, that allow programmable data to be put into the event trailer.

The 48 bit counter derives its 1 usec clock from the VXI 10 MHz clock. The resource manager, in the MTM VXI Mainframe, can initialize the counter to start at a desired value by writing into three 16 bit registers. The counter is always being incremented so as soon as the value is written it will start being incremented. The operator can read back the current state of the counters by reading back the same three 16 bit registers. It is **important** to know that reading back any of the registers in the counter FPGA, while the system is collecting data, may cause invalid data to both the data acquisition system and the VXI interface.

It is also important to know that the significants of the counter bits are different between a read and write. The basic difference between a read and a write is that during a read the MS bit of the middle register has been moved to the upper register.

Relative Address	Write Bit position of Counter Bits	Read Bit position of Counter Bits
0x50	Q15,Q14,Q13,Q12,Q11,Q10,Q09,Q08, Q07,Q06,Q05,Q04,Q03,Q02,Q01,Q00	Q15,Q14,Q13,Q12,Q11,Q10,Q09,Q08, Q07,Q06,Q05,Q04,Q03,Q02,Q01,Q00
0x52	Q31,Q30,Q29,Q28,Q27,Q26,Q25,Q24, Q23,Q22,Q21,Q20,Q19,Q18,Q17,Q16	0, Q30,Q29,Q28,Q27,Q26,Q25,Q24, Q23,Q22,Q21,Q20,Q19,Q18,Q17,Q16
0x54	X, Q46,Q45,Q44,Q43,Q42,Q41,Q40, Q39,Q38,Q37,Q36,Q35,Q34,Q33,Q32	Q46,Q45,Q44,Q43,Q42,Q41,Q40,Q39, Q38,Q37,Q36,Q35,Q34,Q33,Q32,Q31

X = Unused Bit
0 = Always reads zero
Qxx = xx is the bit position of the bits in the 48 bit counter.

The five 16 bit programmable registers, that allow programmable data to be put into the event trailer.

1.3.9 External and Internal TDC

The external and internal TDC each consist of two daughter boards designed and built by LBL. The first module is a time to amplitude conversion daughter board called 23M905 by LBL. The second module is a 12 bit analog to digital daughter board.

The Internal TDC is used to measure the time between the start of the Master Trigger signal and when the next 1 usec tick occurs. By using the 48 bit usec counter, and the internal TDC value, the experimenter can determine with great accuracy (1nsec or better), when an event occurred. Both the Internal TDC value and the usec counter values are given at the end of every event in the event trailer.

The External TDC is used to measure the time between an external pulse and the start of the Master Trigger signal. The external start signal comes into the MTM through a lemo connector on its front Panel. The external start signal is an active low NIM voltage level. The External TDC value can be read at the end of every event trailer.

1.3.10 FASTOUT Data Controller FPGA

The FASTOUT Data Controller (DFCC) FPGA controls how the trailer data is clocked out of the MTM into the event data stream. It monitors when an event has started by detecting when Master-Trigger starts. When the Master-Trigger starts and the Rdy-BsyAB becomes active it drives the RDY-BSY signal to the MRM. The DFCC then waits for the Rdy-BsyAB signal to go low. When the Rdy_BsyAB goes low, if there has been no EOE, the DFCC FPGA moves all of the event trailer data into the Pipeline registers and the Dual Port Ram. A program can poll the data being placed into the event trailer by reading the Dual Port Ram data. Once the data is stored in the pipeline registers the DFCC FPGA then removes its RDY_BSY signal, which notifies the Master Readout Module that the MTM is now ready to be read out. Once all of the RDY_BSY signals to the MRM become inactive, the MRM starts passing around the token. When the MTM receives the token, the DFCC controls how the data is clocks out of its pipeline register. Since the MTM is placed at the end of the token ring its data is always placed at the end of an event. The format of the event trailer is shown below.

Event Trailer

	(EA1)		(EA0)
00000000	External Lemos PT	Module Mult. PT	Ge Mult. PT
00000000	External Lemos MT	Module Mult. MT	Ge Mult. MT
00000000	External Lemos LT	Module Mult. LT	Ge Mult. LT
0000 Internal TAC (From MT to usec tick)		0000 External TAC (From external start to MT)	
0 User Programmable (a)		Usec Counter, bits 31-46	
0 Usec Counter, bits 0-30			
0 User Programmable (b)		User Programmable (c)	
1111 1111	1111 1111	1111 1111	1111 1111

PT = At Pre-Trigger
MT = At Master-Trigger
LT = At Late-Trigger

For a more complete understanding of how the DFCC FPGA works see the schematic of the MTM's Fastout FPGA. This schematic is used as the input to the Xilinx development system and is the ultimate answer to any questions regarding the DFCC FPGA.

1.3.11 Dual Port RAM (DPR)

The Dual Port Ram serves two functions, depending on which mode of operation they are in. In the **normal mode** of operation, the Dual Port RAM receive the same data that goes to the pipeline registers. In this mode the DPR can be used to look at the data being stored in the MTM's pipeline registers. This allows the programmer a way of sampling the event trailer before it gets sent up to the Event Builder. When sampling the DPR data the programmer must realize that the words he reads are probably from different events. There is also a slight possibility that an invalid word could be read if the VXI interface tries to read a word while the DFCC is putting data into the DPR. This is due to the DFCC having priority when accessing the DPR. The format of the data in the DPRs is shown in the tabel below.

Relative Address	Description
0x10	Mod and Ge Sum at Pre-Trigger
0x12	External Lemos at Pre-trigger
0x14	Mod and Ge Sum at Main-Trigger
0x16	External Lemos at Main-trigger
0x18	Mod and Ge Sum at Late-Trigger
0x1a	External Lemos at Late-trigger
0x1c	External TAC
0x1e	Internal TAC
0x110	Usec Counter, bits 31-46
0x112	Programmable 16 Bits (a)
0x114	Usec Counter, bits 0-15
0x116	Usec Counter, bits 16-31
0x118	Programmable 16 Bits (c)
0x11a	Programmable 16 Bits (b)
0x11c	LS Event Trailer - must write 0xffff
0x11e	MS Event Trailer - must write 0xffff

In the **test mode**, the DPR may be used to supply the data that is transfered into the pipeline registers and become the event trailer. This provides a way for the programmer to send any information up to the Event Builder and verify that it was properly transfered.

1.3.12 Pipeline Registers

The Pipeline Register store the sixteen 16 bit words listed in the table above. The data can come from the various devices that supply the event trailer data, or from the DPR, depending on the mode of operation. When the token is passed to the MTM the data in the pipeline registers is transferred over the VXI Local Bus to the Master Readout Module. The data is clocked out of the pipeline registers as eight 32 bit words as shown in the event trailer format above.

1.3.13 VXI Local Bus Interface

The VXI Local Bus Interface consist of bus drivers and receivers used for transferring data over the VXI Local Bus. Four bus drivers are used to transfer the 32 bit words from the Pipeline Registers. Another bus driver is used to drive the TOKEN_OUT, STROBE, and RDY_BSY signals. A bus receiver chip is used to receive the TOKEN_IN signal.

1.3.14 Miscellaneous Circuitry

The Miscellaneous Circuitry on the GeBGO Board consist of glue logic surrounding the FPGAs and the VXI Interface. The main functions performed and controlled by the Miscellaneous Circuitry are Reset, Done, SYSFAIL, DTACK, BERR. Reset is used by the FPGAs to initiate their configuration. On reset each FPGA drives its CCLK signal and loads its configuration from its serial PROM. When an FPGA is finish loading its configuration it releases the Done signal. When all FPGAs are configured the Done signal should go high. The SYSFAIL signal is an open collector signal on the VXI bus. Any board may pull this line low to indicate that it has failed. The GeBGO board will hold this signal low if the Done signal does not go high or if the VXI-INF FPGA holds the signal low. DTACK is a handshaking signal used by the VXI bus. It is controlled by the VXI-INF chip. BERR is also controlled by the VXI-INF and notifies the VXI Master when there has been a bus error.

1.4 Memory Map for MTM

The Master Trigger Module has 512 bytes of address, in A16 address space. The absolute VXI address will be determined dynamically by the Resource Manager. The base addresses of these registers are defined as follows:

A16 ADDRESSING FORMAT
Base Address

11LL LLLH	HH00 0000

L + H = Logical address
L = Bits which are configured during Dynamic Configuration
H = Hard wired (common decode bits for 8 devices/module)

The register definition per Ge/BGO module is:

OFFSET FROM BASE	READ FUNCTION	INITIAL VALUE
00H	ID REGISTER	1111 1111 0000 0000
02H	DEVICE TYPE REGISTER	0000 0000 0000 0000
04H	STATUS REGISTER	xMxx xxxx xxxx 11xx M = MODID BIT
06H	OFFSET REGISTER	0000 0000 0000 1000

OFFSET FROM BASE	WRITE FUNCTION	INITIAL VALUE
00H	LOGICAL ADDRESS REGISTER	xxxx xxxx PPPP Pxxx P = Programmable Bits
02H		
04H		
06H		

Logical Address - used during dynamic configuration to set the Logical Address.
ID Reg - A16 only, For customized device = F00h.
Device Type Reg - 0 bytes of memory, model code = 0.
Status Reg - No A24/A32, Modid active, Ready Passed.
Control Reg - A24/A32 Disabled, Sysfail active, Reset state Off.
Offset Reg - 8 devices (512 bytes) sharing address decoding.

Device	Relative Address	Use	Function	Dev 0 Offset Address
0	000...00f	VXI Configuration Registers	Read ID; Write Logical Address Read Device Type Read Status; Write Control Read/Write Offset Register	000h 002h 004h 006h
0	010...01f	EVENT DATA "A"	Read/Write Event RAM Mod and Ge Pre-Trigger Sum Ext Pretrigger Value Mod and Ge Main-Trigger Sum Ext Main-Trigger Value Mod and Ge Late-Trigger Sum Ext Late-Trigger Value TAC2 Value TAC1 Value	 010h 012h 014h 016h 018h 01ah 01ch 01eh

Device	Relative Address	Use	Function	Dev 0 Offset Address
0	020...02f	Read Status	(Read Only Status Bit) Bit Function 0 - RDY_BSY_IN	020h 022h
		Pretrigger Logic Control (1 enables mask) (0 ingnore input)	(R/W Latch) Bit Function 0 - Ge_AND_Msk 1 - Mod_AND_Msk 2 - Ext_AND_Msk 3 - Ge_OR_Msk 4 - Mod_OR_Msk 5 - Ext_OR_Msk	
		Lookup Table Control (1 selects desired lookup table)	(R/W Latch) Bit Function 0 - 1 Selects Main A0-7 D0-11 Lookup 1 - 1 Selects Main A0-11 D0 Lookup 2 - 1 Selects Late A0-7 D0-11Lookup 3 - 1 Selects Late A0-11 D0 Lookup 4 - 1 Selects Adders to address Lookups 0 Selects VXI to address Lookup Ram.	024h
		Miscellaneous Control	(R/W Latch) 0 - MTM Scalers Reset (0 = Reset) 1 - MTM Scalers Gate (0 = No Counting) 2 - ADC_MEM (1 = ADC mode) 3 - TTL_EN (1 = enable ttl_out -Inhibit) 4 - SOFT A&B	026h
		Lookup Table Address Pointer	R/W Register Auto Increment when there is a Read or write to Lookup Table Data	028h 02ah
		R/W Lookup Table	R/W into the Lookup Table selected by the Lookup Table Control Register at the address selected by the Lookup Table Address Pointer. The Address Pointer is incremented each read or write.	

Device	Relative Address	Use	Function	Dev 0 Offset Address
0	030...03f	Pre-Trigger Pulse Width	Write Latch, Read DPR 8 bit number with 0xFF = 250nsec	030h
		Strobe Pulse Width	Write Latch, Read DPR 8 bit number with 0xFF = 250nsec	032h
		Inhibit Pulse Width	Write Latch, Read DPR 8 bit number with 0xFF = 250nsec	034h
		Delay between Pre-Trigger and Main-Trigger	Write Latch, Read DPR 8 bit number with 0xFF = 1 usec	036h
		Delay between Main and Late Trigger.	Write Latch, Read DPR 8 bit number with 0xFF = 20 usec	038h
		Ge Pre-Trigger Level	Write 8 - Bit DAC, Read DPR 0xFF = 2.5 Volts	03Ah
		Mod Pre-Trigger Level	Write 8 - Bit DAC, Read DPR 0xFF = 2.5 Volts	03Ch

Device	Relative Address	Use	Function	Dev 0 Offset Address
1	040...04f	VXI Configuration Registers	Points to same Registers as Device 0	040h
1	050...05f	1 Usec Counter LS	Write 16 Bits Parallel Load, Read 16 Bits of LS part of Counter	050h
		1 Usec Counter Mid.	Write 16 Bits Parallel Load, Read 15 Bits of Middle part of Counter.	052h
		1 Usec Counter MS	Write 16 Bits Parallel Load, Read 16 Bits with LS bit being MS bit of the Middle section.	054h
		Data Latch for EB1	R/W 16 Bit Data which is put into the event data stream.	056h
		Data Latch for EB4	R/W 16 Bit Data which is put into the event data stream.	058h
		Data Latch for EB5	R/W 16 Bit Data which is put into the event data stream.	05ah
		Data Latch for EB6	R/W 16 Bit Data which is put into the event data stream.	05ch
		Data Latch for EB7	R/W 16 Bit Data which is put into the event data stream.	05eh
1	060...06f	Scratch Memory	Read/Write Dual Port Ram	060h
1	070...07f	Scratch Memory	Read/Write Dual Port Ram	070h

Device	Relative Address	Use	Function	Dev 0 Offset Address
2	080...08f	VXI Configuration Registers	Points to same Registers as Device 0	080h
2	090...09f	Scratch Memory	Read/Write Dual Port Ram	090h
2	0a0...0af	Pre-Trigger Counter	Read 16 MS bits of Scaler 1 Read 16 LS bits of Scaler 1	0a0h 0a2h
		Main-Trigger Counter	Read 16 MS bits of Scaler 2 Read 16 LS bits of Scaler 2	0a4h 0a6h
		Late-trigger Counter	Read 16 MS bits of Scaler 3 Read 16 LS bits of Scaler 3	0a8h 0aah
		Inhibit Counter	Read 16 MS bits of Scaler 4 Read 16 LS bits of Scaler 4	0ach 0aeh
2	0b0...0bf	EOE Counter	Read 16 MS bits of Scaler 5 Read 16 LS bits of Scaler 5	0b0h 0b2h
3	0c0...0cf	VXI Configuration Registers	Points to same Registers as Device 0	0c0h
3	0d0...0df	Scratch Memory	Read/Write Dual Port Ram	0d0h
3	0e0...0ef	Scratch Memory	Read/Write Dual Port Ram	0e0h
3	0f0...0ff	Scratch Memory	Read/Write Dual Port Ram	0f0h

Device	Relative Address	Use	Function	Dev 0 Offset Address
4	100...10f	VXI Configuration Registers	Points to same Registers as Device 0	
4	110...11f	EVENT DATA "B"	Read/Write Event RAM Usec MS 16 bits Programmable 16 bits Usec LS 16 bits Usec Middle 15 bits Programmable 16 bits Programmable 16 bits Programmable 16 bits Programmable 16 bits	 110h 112h 114h 116h 118h 11ah 11ch 11eh
4	120...12f	Scratch Memory	Read/Write Dual Port Ram	120h
4	130...13f	Scratch Memory	Read/Write Dual Port Ram	130h
5	140...14f	VXI Configuration Registers	Points to same Registers as Device 0	
5	150...15f	Scratch Memory	Read/Write Dual Port Ram	150h
5	160...16f	Scratch Memory	Read/Write Dual Port Ram	160h
5	170...17f	Scratch Memory	Read/Write Dual Port Ram	170h

Device	Relative Address	Use	Function	Dev 0 Offset Address
6	180...18f	VXI Configuration Registers	Points to same Registers as Device 0	180h
6	190...19f	Scratch Memory	Read/Write Dual Port Ram	190h
6	1a0...1af	Scratch Memory	Read/Write Dual Port Ram	1a0h
6	1b0...1bf	Scratch Memory	Read/Write Dual Port Ram	1b0h
7	1c0...1cf	VXI Configuration Registers	Points to same Registers as Device 0	1c0h
7	1d0...1df	Scratch Memory	Read/Write Dual Port Ram	1d0h
7	1e0...1ef	Scratch Memory	Read/Write Dual Port Ram	1e0h
7	1f0...1ff	Scratch Memory	Read/Write Dual Port Ram	1f0h

2.0 SCHEMATICS OF MASTER TRIGGER MODULE

3.O SCHEMATIC OF MTM's VXI INTERFACE FPGA

4.0 SCHEMATIC OF MTM'S FASTOUT FPGA

5.0 SCHEMATIC OF MTM's 32-BIT SCALER FPGA

6.0 SCHEMATIC OF MTM's ONE USEC COUNTER FPGA

APPENDIX A: ABEL PROGRAM FOR ECL PALs

APPENDIX B: TEST SOFTWARE

APPENDIX C: DATA SHEETS FOR PARTS USED IN MTM

UTILITY ROUTINES